SEMICONDUCTOR CHIP PACKAGE AND METHOD FOR MANUFACTURING THE SAME

Abstract

A semiconductor chip package mainly comprises an interconnection substrate, a central substrate, a peripheral substrate and a semiconductor chip sandwiched between the interconnection substrate and the central substrate. The interconnection substrate has a recessed cavity for receiving the semiconductor chip. The present invention is characterized in that the peripheral substrate is separated from the central substrate thereby decreasing the stresses caused by CTE mismatch of the semiconductor chip package. Furthermore, both the central substrate and the peripheral substrate are mechanically and electrically connected to the interconnection substrate such that the semiconductor chip is electrically connected to the peripheral substrate through the central substrate and the interconnection substrate. The present invention further provides a method for manufacturing the semiconductor chip package.